

Patent Claims

1. A device (1) for calculating FSM bits (FSM(s)) by means
5 of which the signals sent from two antennas of a base
station are influenced with reference to their phase
difference and/or their amplitudes with the aid of two
estimated channel impulse responses ($h_{1,n}(s)$, $h_{2,n}(s)$),
- the device (1) being present in hard-wired form,
10 - a complex phasor (H_{21}) being formed from components
($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses,
and
- an FSM bit (FSM(s)) being produced by means of rotation
and projection of the phasor (H_{21}) and, in particular, of
15 a threshold value value decision.
2. The device (1) as claimed in claim 1, characterized
- in that components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel
impulse responses can be applied at inputs
20 ($In1$, ..., $In4$) of the device (1),
- in that control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) can be
applied at control inputs (Config1, ..., Config6) of the
device (1), and
- in that the FSM bit (FSM(s)) can be tapped at an output
25 of the device (1), the FSM bit (FSM(s)) being calculated
as a function of the components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the
two channel impulse responses and the control signals
($C_{1,k}(s)$, ..., $C_{6,k}(s)$).
- 30 3. The device (1) as claimed in claim 2, characterized by
- by a logic unit (2, 3) and a processing unit (4, ..., 9)
connected downstream of the logic unit (2, 3).
4. The device (1) as claimed in claim 1, characterized

- in that components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses are present at inputs (In1, In2, In3, In4) of the logic unit (2, 3),
 - in that the logic unit (2, 3) has outputs (Out1, Out2, Out5, Out6) whose number is equal to the number of its inputs (In1, In2, In3, In4), and
 - in that the inputs (In1, In2, In3, In4) of the logic unit (2, 3) can be connected to the outputs (Out1, Out2, Out5, Out6) of the logic unit (2, 3) as a function of at least one of the control signals ($C_{1,k}(s)$, ..., $C_{5,k}(s)$).
5. The device (1) as claimed in claim 3 or 4, characterized
- in that a multiplier stage (4, 5), an adder (6), a weighting stage (7), an accumulator (8) and a threshold value value decision unit (9) are connected in series in the prescribed sequence in the processing unit (4, ..., 9).
6. The device (1) as claimed in claim 5, characterized
- in that the multiplier stage has two multipliers (4, 5) whose inputs are connected in each case to two outputs (Out1, Out2, Out5, Out6) of the logic unit (2, 3), and
 - in that the inputs of the adder (6) are connected to the outputs of the multipliers (4, 5).
7. The device (1) as claimed in claims 5 and 6, characterized
- in that a control signal ($C_{6,k}(s)$) is present at the weighting stage (7), and
 - in that the weighting stage (7) applies a weighting factor to the sum (S_k) formed by the adder (6), doing so as a function of the control signal ($C_{6,k}(s)$) present at it.

8. The device (1) as claimed in one or more of claims 2 to 7, characterized
- in that the control signals are stored in the form of control bits ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) in a read-only memory.
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9. The device (1) as claimed in one or more of the preceding claims, characterized
- in that the device (1) is designed for the UMTS standard.
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10. The device (1) as claimed in claim 9, characterized
- in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of the slot number (s) of the FSM bit (FSM(s)) to be calculated, and of the CLTD mode.
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11. The device (1) as claimed in claim 9 or 10, characterized
- in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of whether the slot number (s) of the FSM bit (FSM(s)) to be calculated is an even or odd number.
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12. A mobile radio terminal having a device (1) as claimed in one or more of the preceding claims.
13. A method for calculating FSM bits (FSM(s)) by means of
- 25 which the signals sent from two antennas of a base station are influenced with reference to their phase difference and/or their amplitudes with the aid of two estimated channel impulse responses ($h_{1,n}(s)$, $h_{2,n}(s)$), having the following steps:
- 30 (a) producing a complex phasor (H_{21}) from components ($h_{1,n}(s)$, $h_{2,n}(s)$) of the two channel impulse responses; and
- (b) calculating an FSM bit (FSM(s)) by rotation and projection of the phasor (H_{21}).

14. The method as claimed in claim 13, characterized
- in that the rotation and projection of the phasor (H_{21}) is determined by control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$).
- 5 15. The method as claimed in claim 13 or 14, characterized
- in that a threshold value value decision is carried out after the rotation and projection of the phasor (H_{21}) in order to calculate the FSM bit ($FSM(s)$).
- 10 16. The method as claimed in one or more of claims 13 to 15, characterized
- in that the method is designed for the UMTS standard.
17. The method as claimed in claims 14 and 16, characterized
15 - in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of the slot number (s) of the FSM bit ($FSM(s)$) to be calculated, and of the CLTD mode.
18. The method as claimed in claim 17, characterized
20 - in that the control signals ($C_{1,k}(s)$, ..., $C_{6,k}(s)$) are a function of whether the slot number (s) of the FSM bit ($FSM(s)$) to be calculated is an even or odd number.